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A. G. Stanley

Analysis of Radiation Effects in Telemetry Circuits

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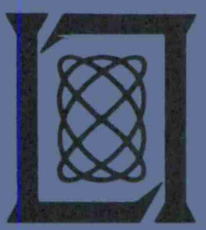
Lexington, Massachusetts



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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

ANALYSIS OF RADIATION EFFECTS IN TELEMETRY CIRCUITS

A. G. STANLEY

Group 63

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LEXINGTON MASSACHUSETTS

ABSTRACT

The effects of nuclear radiation on the telemetry circuits in the LES satellites have been analysed by direct irradiation and by simulating the effects on individual components on a breadboarded circuit. The simulation method is described in detail. It requires a precise knowledge of the behavior of each component operating under specified bias conditions in a radiation environment, but may be applied to circuits of considerable complexity. The analysis confirmed that circuits such as the flip-flop, which operate at 50 per cent duty cycle, are insensitive to moderate leakage currents and have low gain requirements, are extremely radiation resistant. The converse holds for circuits that operate at low duty cycles, that are sensitive to leakage currents and that have more stringent gain requirements.

Accepted for the Air Force
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Lt Colonel, USAF
Chief, Lincoln Laboratory Office

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Analysis of Radiation Effects in Telemetry Circuits

1. INTRODUCTION

Low current switching circuits using bipolar transistors are susceptible to degradation and failure in a nuclear radiation environment produced by a decrease in current gain and by leakage currents across reverse biased junctions. This report considers their effects on the operation of telemetry circuits.

It should be noted that the decrease in current gain and the associated increase in $V_{CE}(sat)$ is a fundamental property of bipolar transistors which may be alleviated by designing circuits with minimal current gain requirements and operating at current levels above 50 μA. On the other hand, radiation induced leakage currents at low bias voltages (less than 10v) may be avoided altogether by screening out defective devices by suitable quality control procedures, e.g., by pre-irradiation with x-rays at a very low total dose.

2. Simulation of Radiation Effects on Breadboarded Circuits

The effect of nuclear radiation on the operation of a circuit may be tested either by direct irradiation or by simulating the effects on a breadboarded circuit. Both methods have their uses, since their advantages and disadvantages complement each other. The simulation method presupposes a thorough knowledge of the behavior of each component under irradiation based on previous experiments. It results in fairly precise design specifications for the circuit in a radiation environment. Direct irradiation of the circuit may be carried

out rapidly and may bring to light unsuspected failure mechanisms. On the other hand, a single circuit under test may not fail at all on account of the statistical nature of many of the effects. It is best, therefore, to use the simulation method for circuit design and the direct irradiation method as a quality control step.

It is easy to simulate bulk damage effects in transistors such as degradation of gain or increase in V_{CE} (sat) by having on hand a collection of devices that have previously been irradiated to a measured total dose. These units are substituted in turn for unirradiated transistors on the breadboard circuit. Some care must be taken to check d-c beta periodically, since there is a long-term annealing effect.

It is more difficult to simulate surface damage, since the effects anneal out rapidly after irradiation. The radiation sensitive components in the telemetry circuits of LES-1 are the 164N2 N-P-N and 172P2 P-N-P silicon planar transistors, which are subject to both bulk and surface degradation. When a P-N-P transistor is irradiated with the base collector junction reverse biased, the p-type collector forms an n-type surface inversion layer at the junction whose electrical characteristics may be represented by a non-linear shunt resistance across the junction. The I-V characteristics are shown in Fig. 1; they are quite typical of inversion layers formed by irradiating planar transistors under bias. Radiation causes the two I_{CBO} curves and the associated I_{CEO} curve (V_C negative) to be displaced along the current axis as the leakage current across the base-collector junction increases. No significant leakage currents were generated across the emitter-base junction. It would

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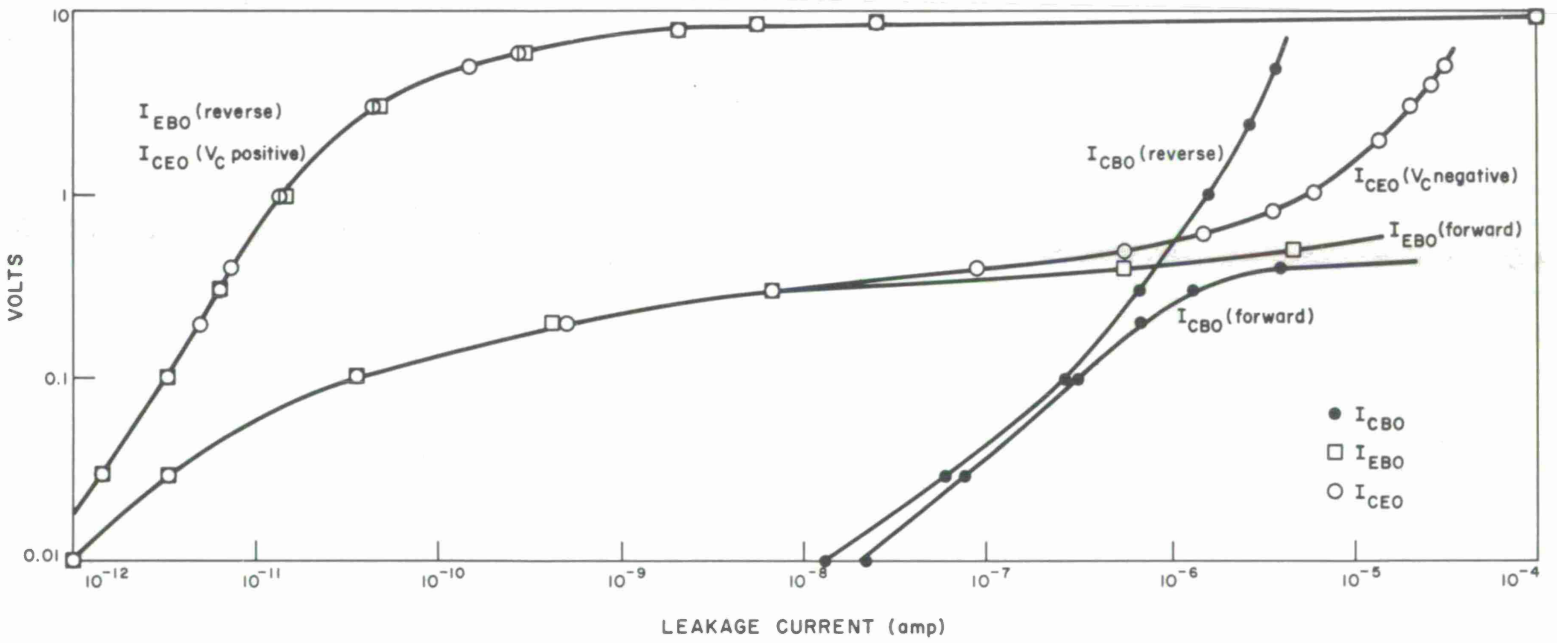

Fig. 1 I-V Characteristics of 172P2 Transistor after Irradiation
Bias During Irradiation: V_{CE} = -6v, I_B = 0

be necessary to irradiate the transistors with the emitter-base junction under reverse bias to develop such leakage currents. This was not done, since it does not correspond to normal transistor operating conditions. In a recent modification of the 172P2 transistor the formation of an n-type inversion layer at the collector surface has been prevented by means of a highly doped p-type guard ring.

The 164N2 transistors that developed significant leakage currents under irradiation produced anomalous I-V characteristics after irradiation (Fig. 2) corresponding to the equivalent circuit shown in Fig. 3. The I_{CEO} vs V_{CE} curves indicate that the leakage paths across the base-collector and base-emitter junctions may be simulated by resistors R_{BC} and R_{BE} which are within the range 10K to 1M. The base lead appears to be connected to the body of the base through a rectifying contact with a capacitance of about 20 pF and a back resistance of about 10^{11} ohms. This equivalent circuit was confirmed by measuring the d. c. and a. c. current gains over the range from 10^{-9} to 10^{-5} amps.

The structure of the 164N2 transistor is shown in Fig. 4. An unusual feature is that the emitter metallization extends over the oxide of the base region forming a metal-oxide-silicon sandwich. The thickness of the oxide is typically 1000 to 2000 Angstroms judging by its interference color. This structure is very susceptible to the formation of inversion layers. All the units that were opened up showed strong evidence of the formation of a gold-silicon-aluminum compound at the bonds know as 'purple plague'. It is believed that this is the cause of the rectifying base contact. The formation of the 'purple plague' on the base lead may have been accelerated by a combination

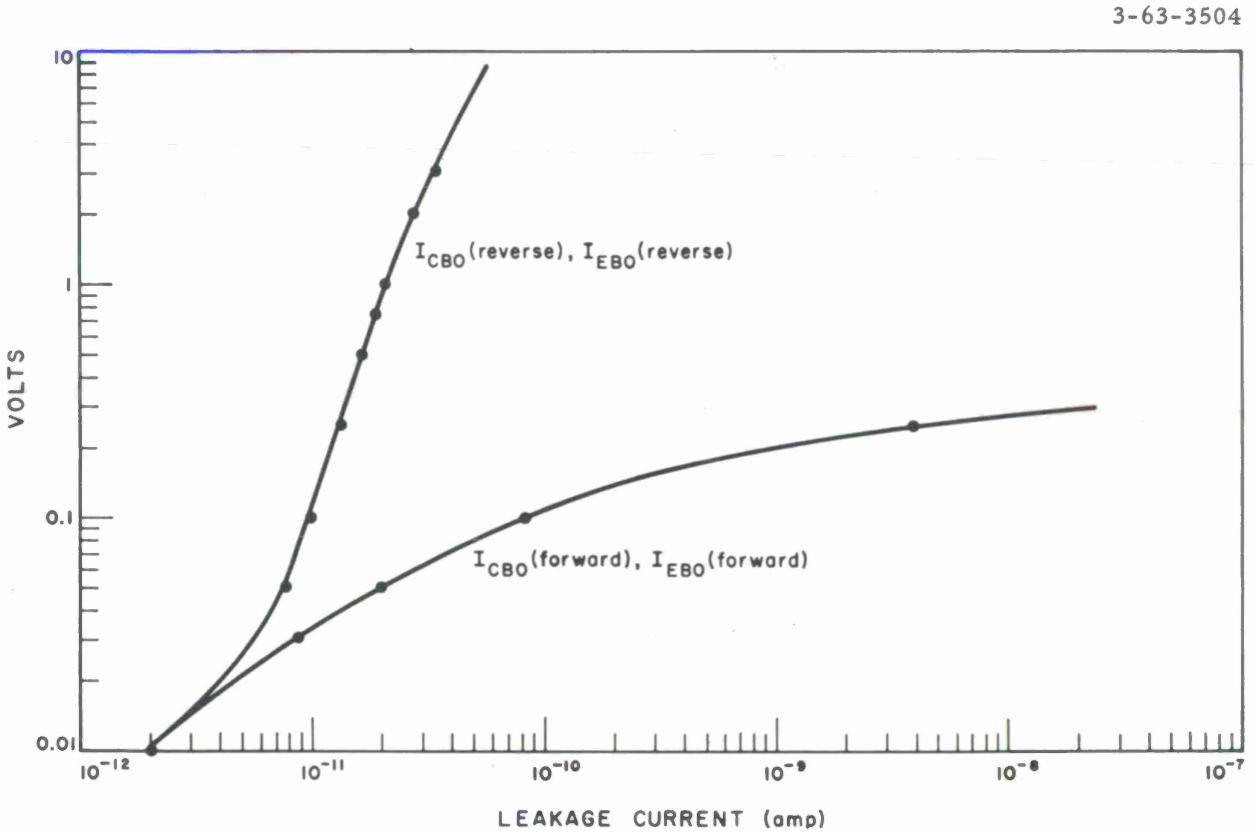

Fig. 2 I-V Characteristics of 164N2 Transistor after Irradiation
Bias During Irradiation: V_{CE} = 6v, I_B = 0

a. I_{CBO} and I_{EBO}

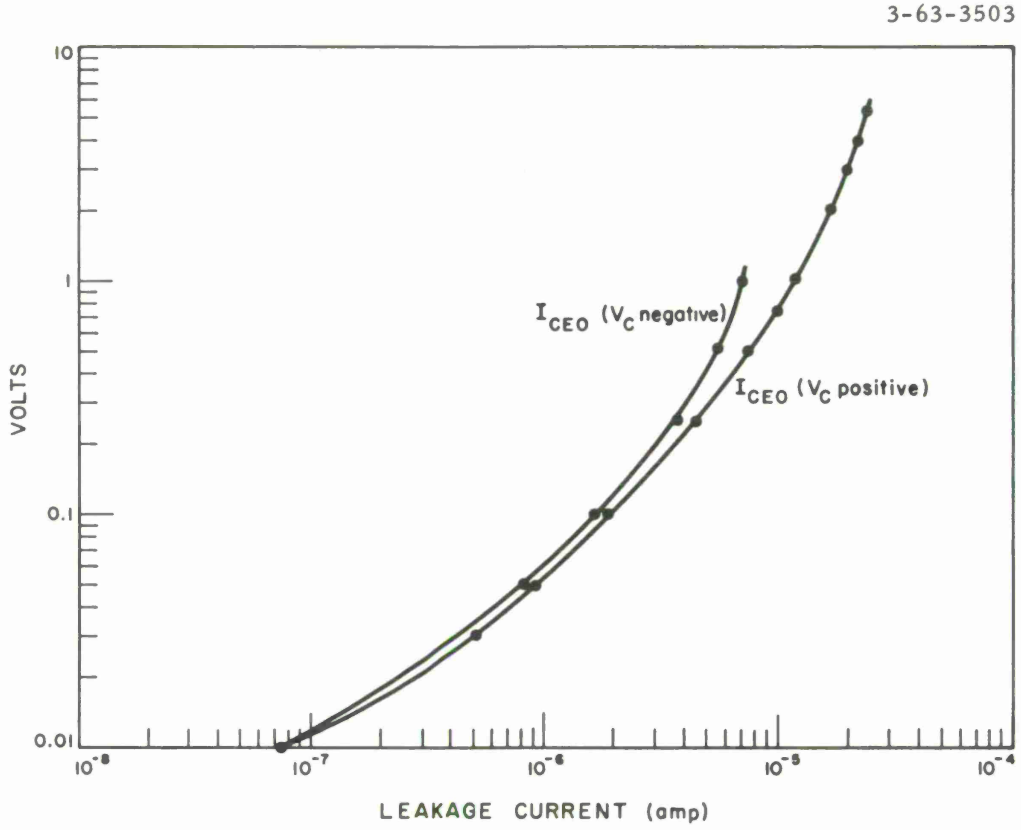

Fig. 2 cont. b. I_{CEO}

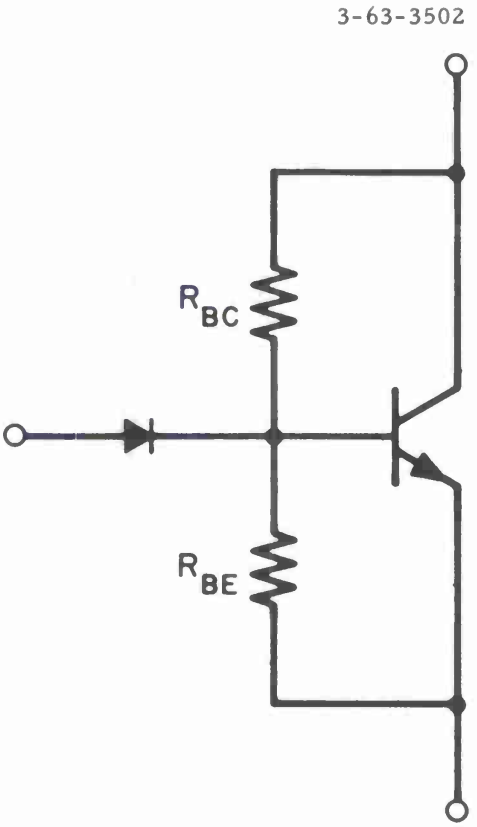

Fig. 3 Equivalent Circuit of Irradiated 164N2 Transistor

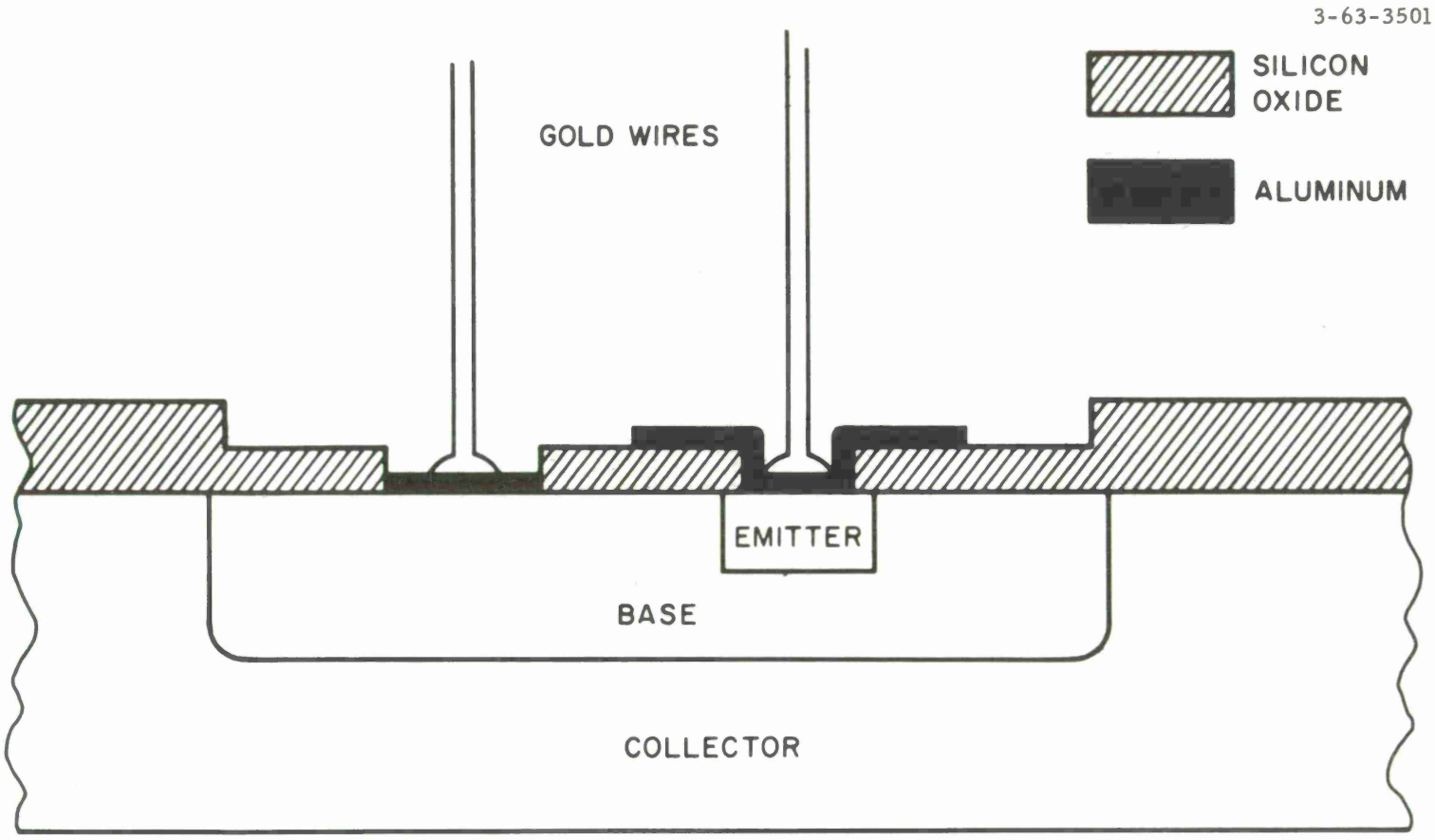

Fig. 4 Structure of 164N2 Transistor
Cross section not drawn to scale

of the irradiation and the passage of substantial leakage currents from emitter to collector for periods of up to eight hours with the base lead open.

The simulation of surface leakage effects is therefore quite complex. As a first order approximation to the problem suitable resistor values were placed in turn in parallel with any two of the three transistor terminals and the effect on the circuit performance was measured. A photo of a breadboarded flip-flop circuit with interchangeable transistors and clip-on resistors is shown in Fig. 5.

3. Inverter

The inverter circuit shown in Fig. 6 is one of the basic telemetry circuits accounting for at least half of all the transistors in the LES telemetry system. On account of its simplicity it was decided to test this circuit directly under electron irradiation and to study the effect of varying the duty cycle on the output current and output voltage. Surface radiation effects are caused by the drift of ions through the oxide under an applied field. Since the drift velocity is quite slow the resulting leakage currents should be strongly dependent on the length of time during which the drift field is applied and hence on the duty cycle.

6v square pulses of different widths were fed into the driver circuit shown in Fig. 6, which was d. c. coupled to the input of the inverter circuit. The load resistor R_L was chosen either as 250K or 2. 2M to represent different loading conditions. I_o, the d. c. current to the collector supply, was measured on a Keithley Micro-microammeter which was connected through a 30 ft.

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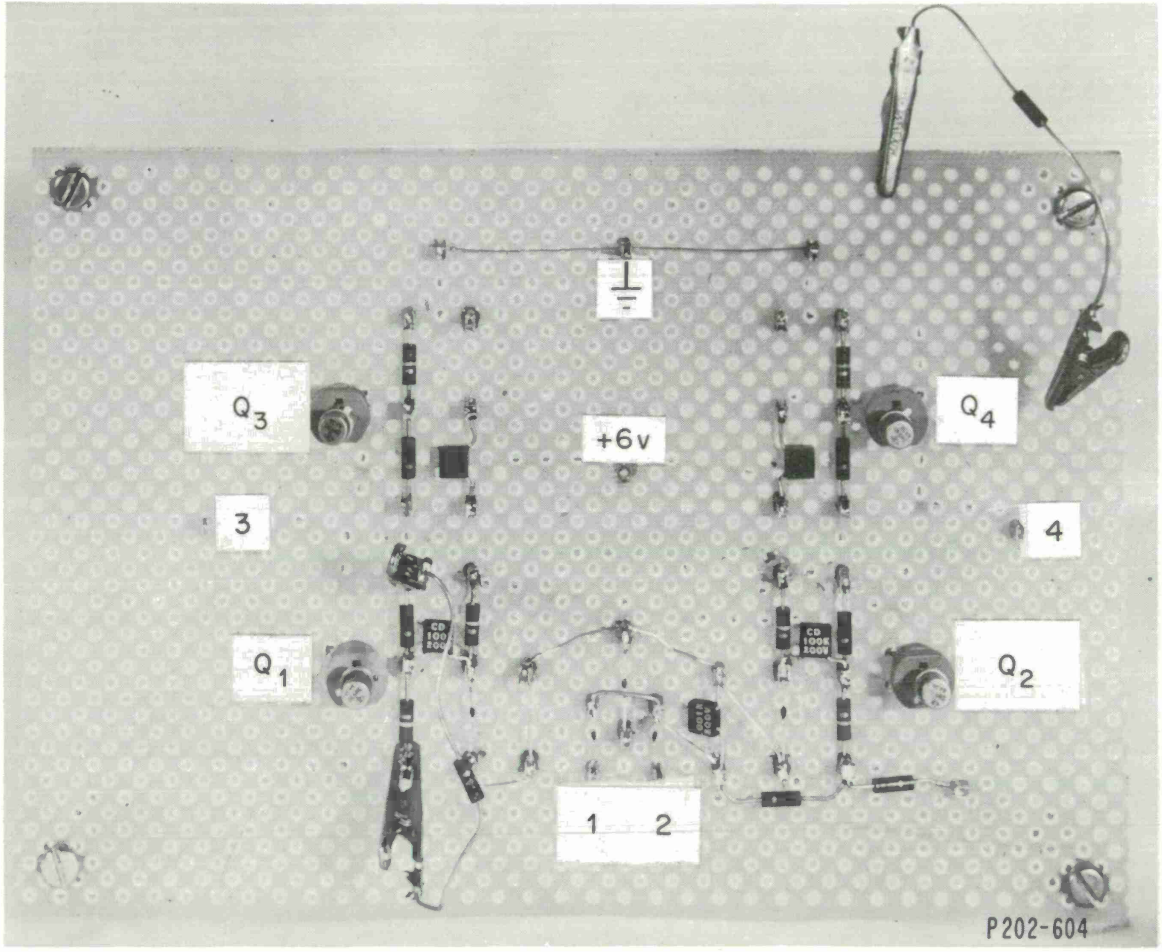

Fig. 5 Breadboarded Flip-Flop Circuit for Radiation Effects Analysis

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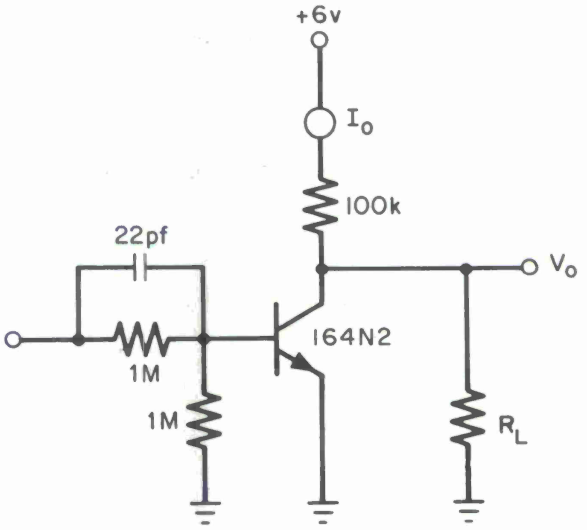

Fig. 6 Inverter

a. Inverter Circuit

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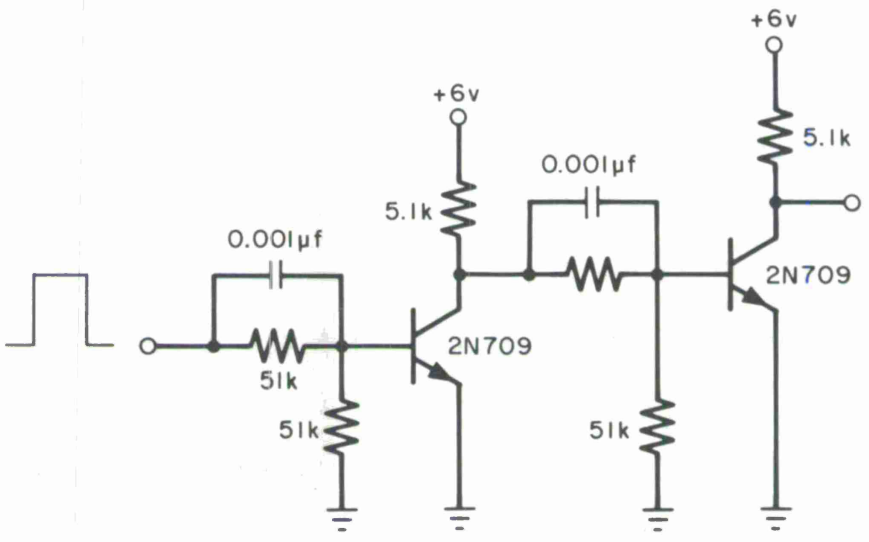

b. Driver Circuit

shielded cable. The output pulse V_o was fed through a high impedance probe to a Tektronix Type 1121 amplifier shielded from the electron radiation and capable of delivering an output pulse through a 30ft. coaxial cable without distortion or attenuation.

The results of the measurements are shown in Table I. The output currents I_o are initially 16.6 and 2.6 μA for 250K and 2.2M loads, respectively, so that collector-emitter leakage currents below these values would not be noticed. The corresponding output voltages V_o are 3.8v and 5v. The circuit is considered to have failed if V_o drops below 3v. It may be seen from the Table that the duty cycle must be greater than 5 per cent for a load resistance of 250K, but that with a load resistance of 2.2M ohms failure occurs only at a duty cycle of 2×10^{-4}. The average duty cycle in the telemetry circuits is 3.12×10^{-2} and the worst case is 7.8×10^{-3}. The pulse width is 80 milliseconds.

4. Analog Voltage Translator

The analog voltage translator circuit shown in Fig. 7 is of sufficient complexity to qualify for the breadboarding technique. A 12v positive pulse, 80 milliseconds long, is applied every 10 seconds to the gate input. The output load, R_L, is represented by a 1M resistor to +6v. A variation of the d. c. level of the analog input is translated into a change in the pulse width of the 6.4v output pulse (see Fig. 8). The circuit is considered to have failed either if the change in the pulse width at the 5v d. c. input level exceeds 2 per cent or if the pulse height decreases to less than 3v.

TABLE I

IRRADIATION MEASUREMENTS ON INVERTER CIRCUITS

	Irradiation Conditions					Initial Values		Values Under Irradiation	
Transistor Unit	Test Cycle On Time sec	Test Cycle Duty Cycle	R_L	Total Dose e/cm^2	Electron Flux $e/cm^2/sec$	Output Pulse V_o	D. C. Output Current I_o μA	Output Pulse V_o	D. C. Output Current I_o μA
E980	ON	1	250K	2.93×10^{14}	1×10^{11}		16.5		16.6
E969	ON	1	250K	2.93×10^{14}	1×10^{11}		16.7		17.0
E967	ON	1	2.2M	2.93×10^{14}	1×10^{11}		2.5		2.6
F185	2.5×10^{-2}	5×10^{-1}	250K	3.49×10^{13}	2.94×10^{8}	3.8v	16.6	3.75v	16.6
F196	2.5×10^{-2}	5×10^{-1}	250K	3.49×10^{13}	2.94×10^{8}	3.8v	16.7	3.5v	17.0
F158	2.5×10^{-2}	5×10^{-1}	2.2M	3.49×10^{13}	2.94×10^{8}	5.0v	2.6	5 v	2.6
F185	2.5×10^{-3}	5×10^{-2}	250K	8.92×10^{13}	2.35×10^{10}	3.8v	16.6	3.5v	20.3
F196	2.5×10^{-3}	5×10^{-2}	250K	8.92×10^{13}	2.35×10^{10}	3.8v	16.7	2.9v	32
F158	2.5×10^{-3}	5×10^{-2}	2.2M	8.92×10^{13}	2.35×10^{10}	5.0v	2.6	5 v	2.8
F195	2.64×10^{-3}	8×10^{-3}	250K	1.73×10^{14}	2.26×10^{10}	3.8v	16.6	1.66v	44
E999	2.64×10^{-3}	8×10^{-3}	2.2M	1.73×10^{14}	2.26×10^{10}	5 v	2.6	3.85v	22
F160	2.64×10^{-3}	8×10^{-3}	2.2M	1.73×10^{14}	2.26×10^{10}	5 v	2.6	3.8 v	26
F195	1×10^{-4}	2×10^{-4}	250K	8.92×10^{13}	2.35×10^{10}	3.8v	16.6	1.5 v	46
E999	1×10^{-4}	2×10^{-4}	2.2M	8.92×10^{13}	2.35×10^{10}	5.0v	2.6	3.5v	25.2
F160	1×10^{-4}	2×10^{-4}	2.2M	8.92×10^{13}	2.35×10^{10}	5.0v	2.6	2.5v	33
F195	1×10^{-6}	2×10^{-6}	250K	3.49×10^{13}	2.94×10^{8}	3.8v	16.6	1.5v	41
E999	1×10^{-6}	2×10^{-6}	2.2M	3.49×10^{13}	2.94×10^{8}	5.0v	2.6	3.5v	18.4
F160	1×10^{-6}	2×10^{-6}	2.2M	3.49×10^{13}	2.94×10^{8}	5.0v	2.6	2.5v	28
F072	OFF	0	250K	8.92×10^{13}	2.35×10^{10}		16.7		30
F056	OFF	0	2.2M	8.92×10^{13}	2.35×10^{10}		2.64		30
F197	OFF	0	2.2M	8.92×10^{13}	2.35×10^{10}		2.6		22.7

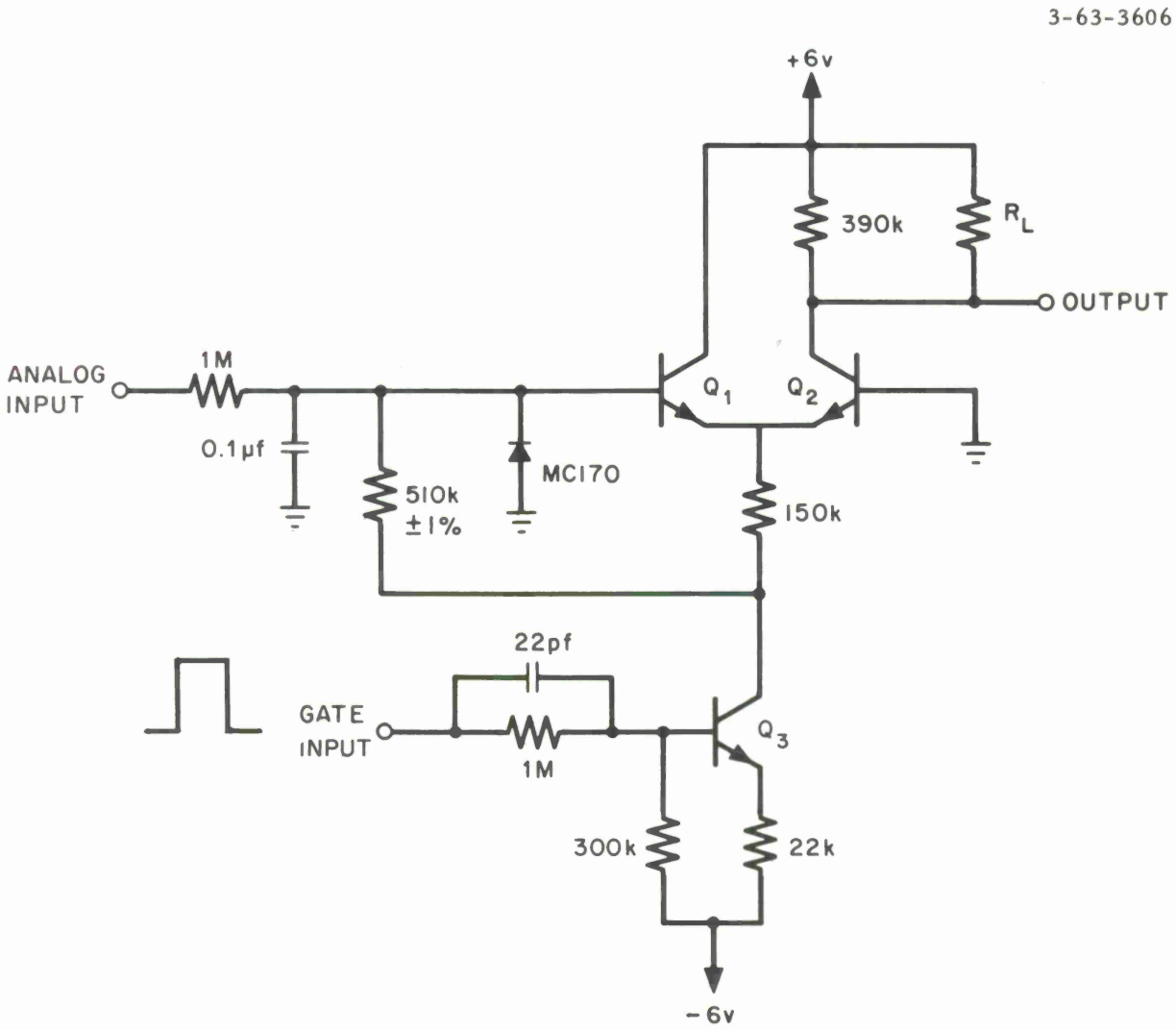

Fig. 7 Analog Voltage Translator

The results of the measurements are shown in Table II. The pulse width of the output pulse is very sensitive to the gain of transistor Q_1, which increases as the gain decreases (see Fig. 8). Changes in the gain of Q_2 and Q_3 have no effect on the output pulse.

The three 164N2 transistors used in the translator circuit may develop leakage currents across the emitter-collector terminals and also across the base-emitter and base-collector junctions. Small leakage currents below 1 μA produce changes in the width of the output pulse; larger leakage currents cause the pulse to decrease in voltage and ultimately to disappear. These effects are enhanced by the low duty cycle of the circuit.

5. Flip Flop

The flip flop circuit shown in Fig. 9 was also subjected to the breadboarding technique. A 6v negative pulse, 80 milliseconds long, is applied every 10 seconds to either inputs 1 or 2. The load impedances R_L are represented by 250K resistors to ground. The output signal is normally either 5.8v or 0.05v. The circuit is considered to have failed if these values change to less than 5v and greater than 1v, respectively.

The results of the measurements are shown in Table III. The circuit still operates with transistors whose d.c. gain is less than 5 and requires very large leakage currents to put it out of action. The detailed operation of this circuit is described in Ref. 1. The circuit will not fail as long as sufficient base current is available to drive the transistors. Furthermore, a build-up of large leakage currents is unlikely with a 50 per cent duty cycle.

TABLE II

SIMULATED RADIATION EFFECTS ON ANALOG VOLTAGE TRANSLATOR

Analog Input: = 5v d. c.
Output Load: R_L = 1

A. Effect of D. C. Gain

Transistor	D. C. Gain At		Q_1		Q_2		Q_3	
	I_c = 5μ A	I_c = 50μ A	Output Volts	Pulse Width in msec	Output Volts	Pulse Width in msec	Output Volts	Pulse Width in msec
29	13	35	6.4	37	6.4	32.5	6.4	32.5
31	8.1	21	6.4	39	6.4	32.5	6.4	32.5
33	5.6	14.7	6.4	42	6.4	32.5	6.4	32.5
Unirradiated	50-100	80-160	6.4	32.5	6.4	32.5	6.4	32.5

TABLE II (continued)

SIMULATED RADIATION EFFECTS ON ANALOG VOLTAGE TRANSLATOR

Analog Input: = 5v d. c.
Output Load: R_L = 1

B. Effect of Leakage Currents

Shunt Resistance	Leakage Current	Output Volts	Pulse Width in msec	Leakage Current	Output Volts	Pulse Width in msec	Leakage Current	Output Volts	Pulse Width in msec
				1. EMITTER-COLLECTOR					
∞	0	6.4	32.5	0	6.4	32.5	0	6.4	32.5
50M							10nA	6.4	33.5
20M							25nA	6.4	35
10M	730nA	6.4	32.5	20nA	6.4	32.5	50nA	6.4	39
1M	7.3μA	6.1	31	200nA	5.4	32.5	500nA	6.4	39
500K	14.6μA	4.2	31	400nA	5.0	32.5	1μA	6.4	40
200K	36.5μA	0	--						
100K				2μA	1.0	32.5	5μA	1.9	80
				2. EMITTER-BASE					
∞	0	6.4	32.5	0	6.4	32.5	0	6.4	32.5
50M				65nA	6.4	32.7			
20M				260nA	6.4	34			
10M	20nA	6.4	32.5	130nA	6.4	35			
1M	200nA	6.4	35.5	1.3μA	6.4	37.5			
500K	400nA	6.4	38.5				1.2μA	6.4	32.5
200K	1μA	6.4	44				3 μA	6.4	29.5
100K	2μA	6.4	55	13μA	6.4	39.5	6 μA	0	----
				3. BASE-COLLECTOR					
∞	0	6.4	32.5	0	6.4	32.5	0	6.4	32.5
20M	355nA	6.4	31.0				55nA	6.4	35.5
10M	710nA	6.4	29.5	110nA	6.3	32.5	110nA	6.4	37.5
5M	1.42μA	6.4	25.0				220nA	6.4	40.5
1M	7.1μA			1.1μA	5.4	32.5	1.1μA	6.4	72
500K				2.2μA	4.4	32.5	2.2μA	2.0	80
200K				5.5μA	2.8	31.5	5.5μA	0	----
100K				11μA	2.0	31.0			

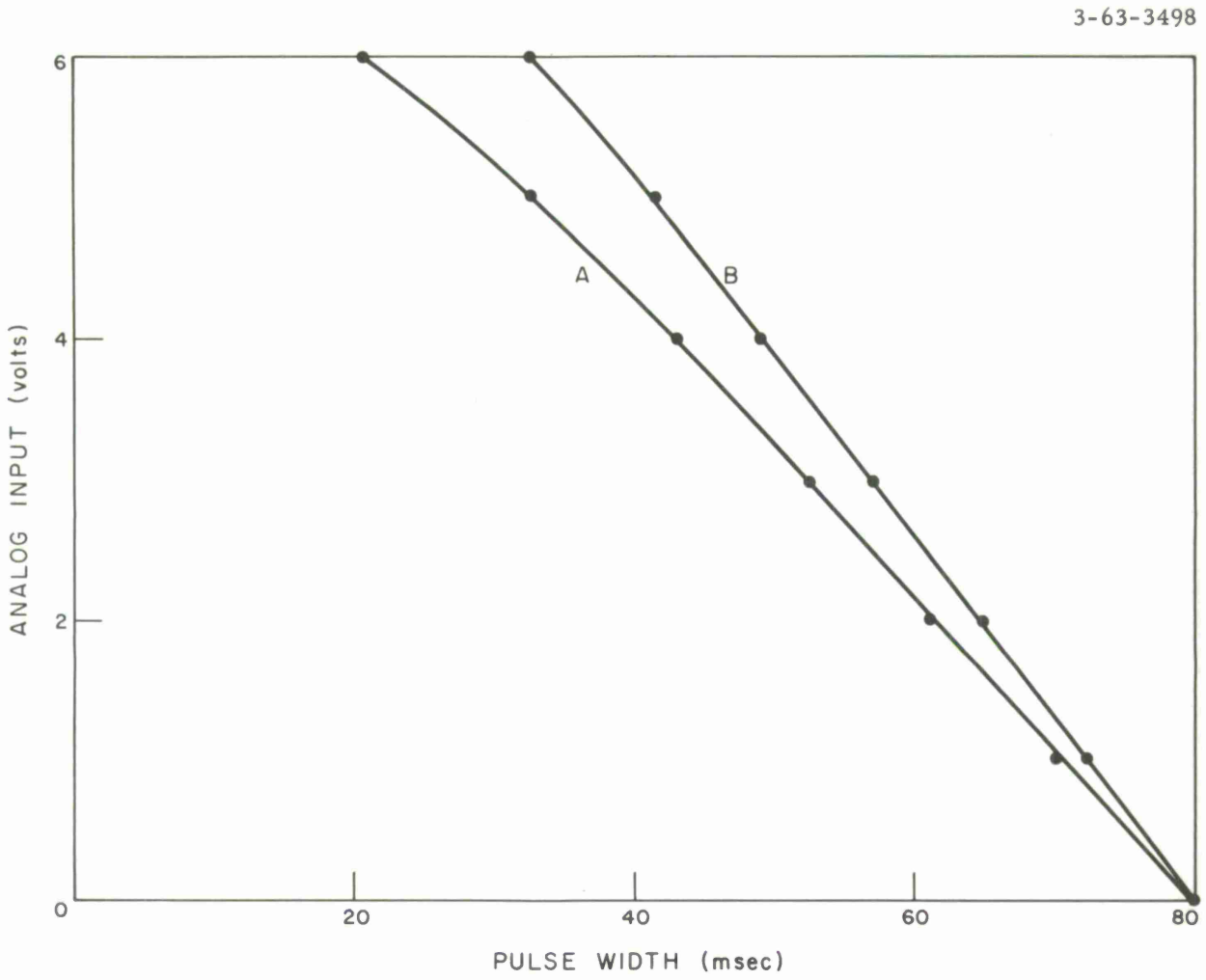

Fig. 8 D. C. Analog Input Voltage vs. Output Pulse Width

Curve A: Unirradiated Transistors

Curve B: Irradiated Transistor with D. C. Gain of 5.6 at $I_c = 5\mu$ A in Position Q_1

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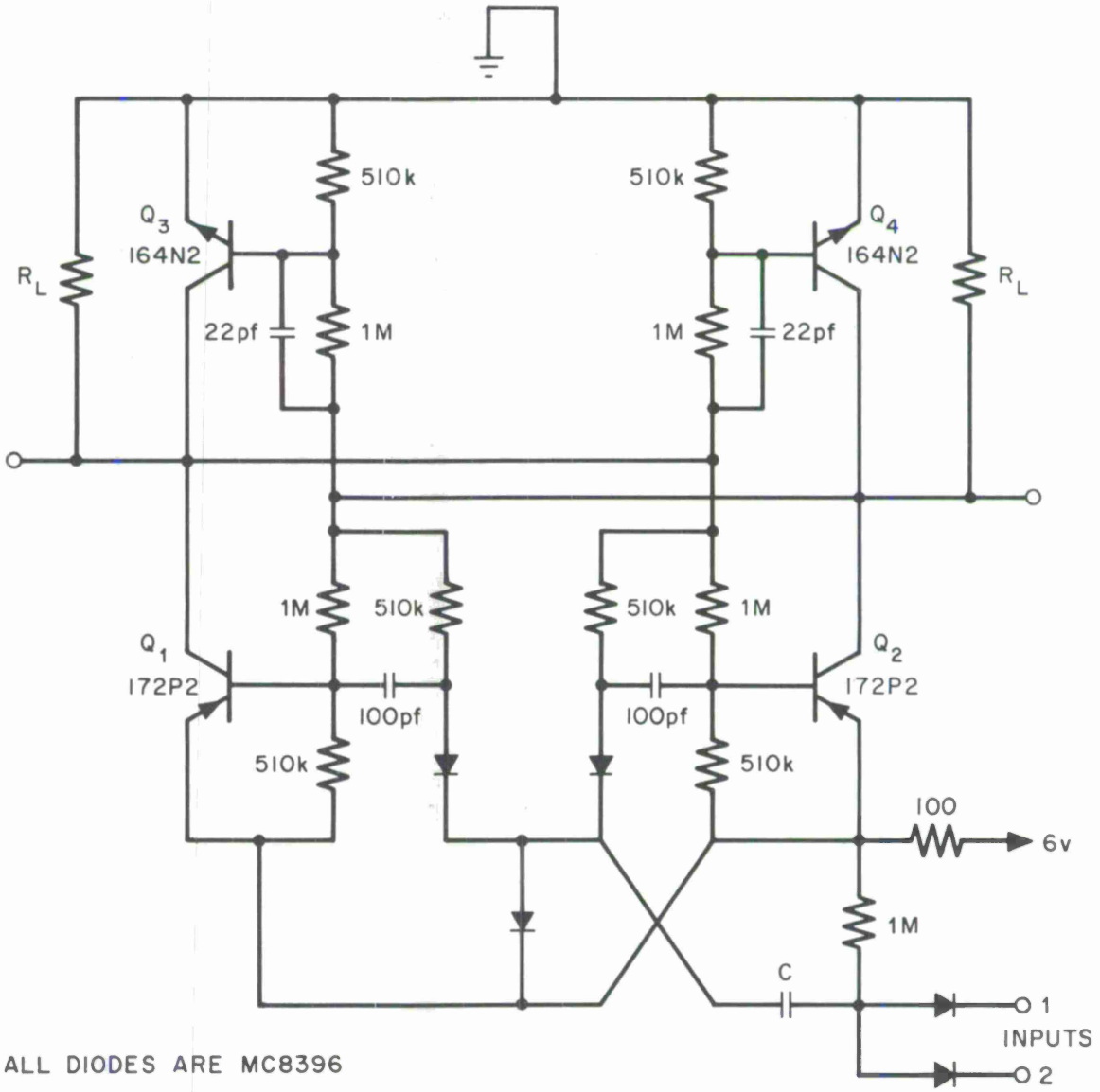

ALL DIODES ARE MC8396

C = LOW FREQUENCY 1000pf
HIGH FREQUENCY 430 pf

Fig. 9 Flip-Flop Circuit

TABLE III

SIMULATED RADIATION EFFECTS ON FLIP FLOP

Output Load: R_L = 250K

A. Effect of D. C. Gain

	D.C. Gain at $I_c = 5\mu A$	D.C. Gain at $I_c = 50\mu A$	Type	Position in Circuit	Transistor On	Transistor Off
Radiated	4.76	8.3	172P2	Q_1 or Q_2	5.8v	0.05v
Unirradiated	20-100	50-150	172P2	Q_1 or Q_2	5.8v	0.05v
Radiated	5.6	14.7	164N2	Q_3 or Q_4	0.05v	5.8v
Unirradiated	50-150	100-200	164N2	Q_3 or Q_4	0.05v	5.8v

TABLE III (continued)

SIMULATED RADIATION EFFECTS ON FLIP FLOP

B. Effect of Leakage Currents

Shunt Resistance	Q_1 or Q_2 172P2				Q_3 or Q_4 164N2			
	ON		OFF		ON		OFF	
	Leakage Current	Output Voltage	Leakage Current	Output Voltage	Leakage Current	Output Voltage	Leakage Current	Output Voltage
				1. EMITTER-COLLECTOR				
∞	0	5.8v	0	0.05v	0	0.05v	0	5.8v
100K	2μA	5.8v	60μA	0.15v	0	0.05v	58μA	5.8v
50K					0	0.05v	116μA	5.8v + tail
20K					0	0.05v	290μA	4.6v
10K	20μA	5.9v	600μA	0.2v	0	0.05v	580μA	0
				2. EMITTER-BASE				
∞	0	5.8v	0	0.05v	0	0.05v	0	5.8v
200K	1.2μA	5.8v	0.5μA	0.05v				
100K	6 μA	0.05v	1 μA	0.05v	5μA	0.8v	2μA	5.8v
50K					10μA	1.2v	4μA	5.8v
10K					50μA	5.9v	20μA	5.9v
				3. BASE COLLECTOR				
∞	0	5.8v	0	0.05	0	0.05	0	5.8v
100K	4μA	5.8v	59μA	0.05	5μA	0.05	56μA	5.8v
50K	8μA	erratic pulse	118μA	erratic pulse	10μA	0.05	112μA	0.05v

6. Conclusion

Table IV summarizes the failure modes of the different telemetry circuits. This includes the clock circuit (Fig. 10) whose failure mode was not verified experimentally. The flip-flops and also the clock circuit are very radiation resistant thanks to the 50 per cent duty cycle and the low gain requirements. At the other extreme, the analog voltage translators are very sensitive to radiation due to a combination of low duty cycle, sensitivity to low leakage currents and one transistor position with a moderately high gain requirement. The inverters are affected by leakage currents of about 20μ A and also have a low duty cycle.

The technique for simulating radiation effects described in this memo should be applicable to circuits of considerably greater complexity.

TABLE IV

SUMMARY OF RESULTS

Circuit	Sensitive Component		Duty Cycle	Gain	Failure Mode: Leakage Current E-C	E-B	B-C
Clock	$Q_1 + Q_2$:	172P2	50 %	5 at 50μA	20μA		
	Q_3 :	164N2	50 %	10 at 50μA	25μA		
	Q_4 :	172P2	50 %	10 at 50μA	25μA		
Flip-Flops	$Q_1 + Q_2$:	172P2	50 %	<5 at 5μA		6μA	8μA
	$Q_3 + Q_4$:	164N2	50 %	<5 at 5μA	300μA	10μA	100μA
Inverters		164N2	0.8%, 3.1%	10 at 60μA	20μA		
		172P2	0.8%, 3.1%	10 at 60μA	20μA		
Analog Voltage Translators	Q_1 :	164N2	0.8%	>15 at 5μA	5μA	200nA	400nA
	Q_2 :	164N2	0.8%	< 5 at 5μA	2μA	100nA	5μA
	Q_3 :	164N2	0.8%	< 5 at 5μA	10nA	3μA	50nA

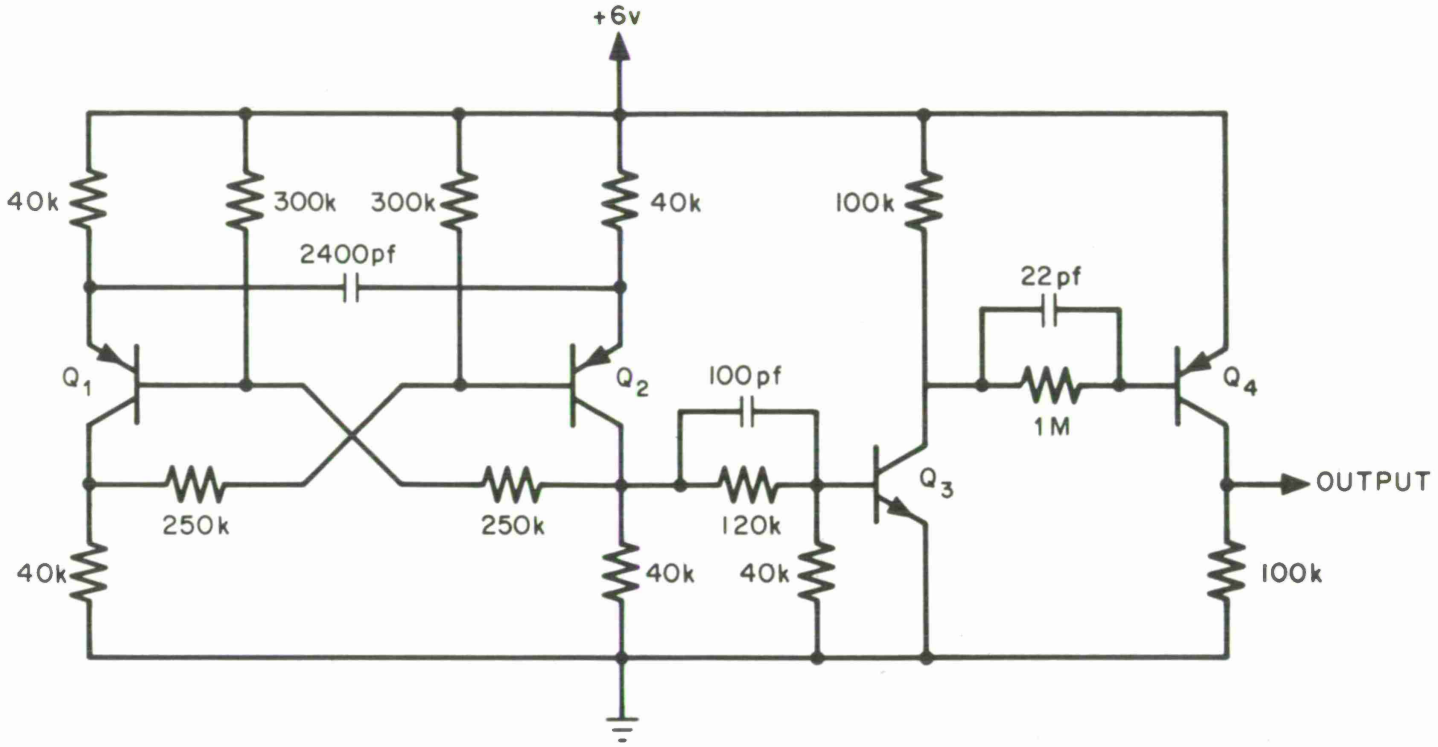

Fig. 10 Clock Circuit

REFERENCES

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The effects of nuclear radiation on the telemetry circuits in the LES satellites have been analyzed by direct irradiation and by simulating the effects on individual components on a breadboarded circuit. The simulation method is described in detail. It requires a precise knowledge of the behavior of each component operating under specified bias conditions in a radiation environment, but may be applied to circuits of considerable complexity. The analysis confirmed that circuits such as the flip-flop, which operate at 50 percent duty cycle, are insensitive to moderate leakage currents and have low gain requirements, are extremely radiation resistant. The converse holds for circuits that operate at low duty cycles, that are sensitive to leakage currents and that have more stringent gain requirements.

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